CLAIMS

1. A method of producing a semiconductor device, including:

a step of depositing organic based interlayer insulation films (4, 6);

a step of forming an opening portion on the organic based interlayer insulation films (4, 6); and

a step of performing silylation to reform a wall surface portion of the organic based interlayer insulation films (4, 6) exposed in said opening portion.

2. A method of producing a semiconductor device according to claim 1, characterized by further including a step of forming protective layers (4b, 6b) including an inorganic based insulation material on a surface of said opening portion wall surface subjected to silylation.

3. A method of producing a semiconductor device according to claim 2, characterized that the inner wall surface of said opening portion including silylated molecules as a result of silylation is exposed to oxide plasma to form a silicon oxide film for protecting the inner wall of the opening portion in a step of forming said protective films (4b, 6b).

4. A method of producing a semiconductor device according to claim 1, characterized by further including

a step of forming an organic based substance in a state of being formed with said opening portion and removing the organic based substance at least from said opening portion after said silylation.

5. A method of producing a semiconductor device according to claim 4, characterized that

said opening portion comprises a via hole (VH) formed by penetrating two interlayer insulation films (4, 6) in a dual damascene wiring process; and

a step of forming a wiring trench (CG) connected to said via hole (VH) on an upper interlayer insulation film (6) of said two interlayer insulation films (4, 6) through the steps of coating a photo resist (R) and performing exposure and development in a state of being formed with the via hole (VH) is further included.

6. A method of producing a semiconductor device according to claim 5, characterized by further including a step of forming an etching stopper film (5) for protecting a via hole (VH) on a lower interlayer insulation film (4) of said two interlayer insulation films (4, 6) in advance between said two interlayer insulation films (4, 6) when etching for forming said wiring trench (CG).

7. A method of producing a semiconductor device according to claim 6, characterized that said etching

stopper film (5) comprises a silicon nitride film.

8. A method of producing a semiconductor device according to claim 5, characterized that at least said upper layer interlayer insulation film (6) formed with said wiring trench (CG) of said two interlayer insulation films (4, 6) include an organic based insulation material.

9. A method of producing a semiconductor device according to claim 8, characterized that said organic based insulation material is any one of a methyl group-containing SiO_2 film, a polyimide based polymer film, a parylene based polymer film, a Teflon (registered trademark) based polymer film, a poly aryl ether based polymer film and an amorphous carbon film doped with fluorine.

10. A method of producing a semiconductor device according to claim 1, characterized by forming a porous organic insulation film as said organic based interlayer insulation films (4, 6).

11. A method of producing a semiconductor device including a step of forming an opening portion on organic based interlayer insulation films (4, 6), including:

a step of depositing organic based interlayer insulation films (4, 6) containing a silylating agent;

a step of forming an opening portion on the organic based interlayer insulation films (4, 6); and

a step of forming protective layers (4b, 6b) comprise an inorganic based interlayer insulation material on an inner wall surface of said opening portion containing a silylating agent.

12. A method of producing a semiconductor device according to claim 11, characterized that said protective film comprises silicon oxide.

13. A method of producing a semiconductor device according to claim 11, characterized that an silicon oxide film for protecting an inner wall surface of the opening portion is formed by exposing the inner wall surface of said opening portion containing a silylating agent to oxygen plasma in a step of forming said protective films (4b, 6b).

14. A semiconductor device, comprising two organic based interlayer insulation films (4, 6) stacked on top of another, wherein a via hole (VH) is formed on a lower layer interlayer insulation film (4) and a wiring trench (CG) connected to said via hole (VH) is formed on an upper layer interlayer insulation film (6) of the two organic based interlayer insulation films (4, 6), and having a wiring configuration that a conductive material (9, 10) is buried in the wiring trench (CG) and said via hole (VH); wherein

an inner wall portion of said via hole (VH)

of a lower layer interlayer insulation film (4) of said two interlayer insulation films (4, 6) is provided with a silylated molecules containing layer (4a) and a protective layer (4b) includes an inorganic based insulation substance formed on a via hole (VH) inner wall surface portion of the silylated molecules containing layer (4a).

15. A semiconductor device according to claim 14, characterized that said protective layer (4b) comprises silicon oxide.

16. A semiconductor device according to claim 14, characterized that said opening portion comprises a via hole (VH) formed by penetrating two interlayer insulation films (4, 6) in a dual damascene wiring process.

17. A semiconductor device according to claim 14, characterized that an etching stopper film (5) for protecting a via hole (VH) of a lower layer interlayer insulation film (4) of said two interlayer insulation films (4, 6) is formed between said two interlayer insulation films (4, 6).

18. A semiconductor device according to claim 14, characterized that said etching stopper film (5) comprises a silicon nitride film.

19. A semiconductor device according to claim 14,

characterized that an organic based insulation material composing said two interlayer insulation films (4, 6) is any one of a methyl group-containing SiO_2 film, a polyimide based polymer film, a parylene based polymer film, a Teflon (registered trademark) based polymer film, a poly aryl ether based polymer film and an amorphous carbon film doped with fluorine.

20. A semiconductor device according to claim 14, characterized that said two organic based interlayer insulation films (4, 6) comprise a porous organic insulation film.